DDR4 UDIMM

BASE ON 8Gb

REVISION HISTORY

Revision No.	History	Draft Date	Editor
1.0	Initial Release	2025.7.4	Yang

TABLE OF CONTENTS

1. FEATURES..... 4

2. DDR4 UNBUFFERED DIMM ORDERING INFORMATION..... 4

3. KEY FEATURES..... 5

4. ADDRESS CONFIGURATION..... 5

5. UNBUFFERED DIMM PIN CONFIGURATIONS (Front side/Back side)..... 6

6. PIN DESCRIPTION.....7

7. INPUT/OUTPUT FUNCTIONAL DESCRIPTION.....8

8. DQ MAPS..... 10

9. FUNCTION BLOCK DIAGRAM.....11

10 ABSOLUTE MAXIMUM RATINGS..... 12

11 AC & DC OPERATING CONDITIONS.....12

12 SPD EEPROM OPERATING CONDITION.....14

13 PHYSICAL DIMENSIONS..... 15

For More Information..... 15

1. FEATURES

- 288-pin, dual in-linememory module (UDIMM)
- Data transfer rates: 2400Mbps/2666Mbps/3200Mbps
- 8GB (1024Mx1x64)
- V_{DD}=1.20V(NOM)
- V_{PP}=2.5V(NOM)
- V_{DDSPD}=2.5V(NOM)
- Nominal and dynamic on-die termination(ODT)
- Programmable Partial Array Self-Refresh (PASR)
- Databus inversion(DBI) for data bus
- On-die V_{REFDQ} generationandcalibration
- Single-rank
- On-board I^2C serial presence-detect(SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop(BC) of 4 and burst length(BL) of 8 via themode registerset(MRS)
- Selectable BC4 or BL8 on-the-fly(OTF)
- Gold edge contacts
- RoHS compliant
- Fly-by topology
- Terminated control commandand address bus
- Commercial(0°C≤ T_{OPER} ≤ 70°C)
- 0.83ns@ CL =17 (DDR4-2400)/0.75ns@ CL =19 (DDR4-2666)/0.625ns@ CL =24 (DDR4-3200)

2. DDR4 UNBUFFERED DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Number of Rank	Organization	Density	Data Rate	Temp Sensor	Height	Environment
1	1Gx1x64（1Rx4）	8GB	2400 Mbps	No	30mm	Commercial
1	1Gx1x64（1Rx4）	8GB	2666 Mbps	No	30mm	Commercial
1	1Gx1x64（1Rx4）	8GB	3200 Mbps	No	30mm	Commercial

3. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	17-17-17	19-19-19	21-21-21	24-22-22	
tCK(min)	0.833	0.75	0.682	0.625	ns
CAS Latency	17	19	21	24	nCK
tRCD(min)	14.16	14.25	14.32	13.75	ns
tRP(min)	14.16	14.25	14.32	13.75	ns
tRAS(min)	32	32	32	32	ns
tRC(min)	46.16	46.25	46.32	45.75	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- VDDQ = 1.2V ± 0.06V
- Bi-directional Differential Data Strobe
- Average Refresh Period 7.8us at lower then T_{CASE} 85℃, 3.9us at 85°C < T_{OPER} ≤ 95°C.

4. ADDRESS CONFIGURATION

[Table 3] address configuration

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
1048Mx4(8Gb)	A0-A15	A0-A9	BG0-BG1	BA0-BA1	A10/AP

5. UNBUFFERED DIMM PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	DM3_n,DBI3_n, NC	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	NC	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	DM0_n,DBI0_n, NC	151	VSS	45	DQ26	189	VSS	82	RAS_n/A16	226	VDD	120	VSS	264	DQ49
8	NC	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	RFU	121	DM6_n,DBI6_n, NC	265	VSS
9	VSS	153	DQS0_t	47	CB4, NC	191	VSS	84	CS0_n	228	WE_n/A14	122	NC	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5, NC	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0, NC	193	VSS	86	CAS_n/A15	230	NC	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1, NC	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	DM8_n,DBI8_n, NC	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	NC	196	DQS8_c	89	CS1_n	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	NC	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6, NC	198	VSS	91	ODT1	235	NC	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7, NC	92	VDD	236	VDD	130	DQ56	274	VSS
18	DM1_n,DBI1_n, NC	162	VSS	56	CB2, NC	200	VSS	93	NC	237	NC	131	VSS	275	DQ57
19	NC	163	DQS1_c	57	VSS	201	CB3, NC	94	VSS	238	SA2	132	DM7_n,DBI7_n, NC	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	NC	277	DQS7_c
21	DQ14	165	VSS	59	VDD	203	CKE1	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS
23	DQ10	167	VSS	61	VDD	205	RFU	98	VSS	242	DQ33	136	VSS	280	DQ63
24	VSS	168	DQ11	62	ACT_n	206	VDD	99	DM4_n,DBI4_n, NC	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	NC	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS
27	DQ16	171	VSS	65	A12/BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	DM2_n,DBI2_n, NC	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	NC	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	RFU	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45				
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	DM5_n,DBI5_n, NC	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	NC	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

6. PIN DESCRIPTION

[Table 4] pin description

Pin Name	Description
A0–A17[1]	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n[2]	SDRAM row address strobe
CAS_n[3]	SDRAM column address strobe
WE_n[4]	SDRAM write enable
CS0_n, CS1_n	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.Not used on UDIMMs.
DQS0_t–DQS8_t	SDRAM data strobes (negative line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x64 DIMMs)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
SCL	I2C serial bus clock for SPD-TSE
SDA	I2C serial bus data line for SPD-TSE
SA0–SA2	I2C slave address select for SPD-TSE
PARITY	SDRAM parity input
VDD	SDRAM I/O and core power supply
12 V	Optional power Supply on socket but not used on UDIMM
VREFCA	
VSS	Power supply return (ground)
VDDSPD	Serial SPD-TSE positive power supply
ALERT_n	SDRAM ALERT_n
VPP	SDRAM Supply
RESET_n	Set DRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :

1) Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

7. INPUT/OUTPUT FUNCTIONAL DESCRIPTION

[Table 5] Input/Output function description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
ODT (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disableRTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/ DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. TDQS is not valid for UDIMMs.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normaloperation.

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t,DQS_c, DQSU_t,DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0- BG1, BA0-BA1, A16-A0. LOW Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n islow.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system.
TEN	Input	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistorto VSS
NC		No Connect: No on DIMM electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
12 V	Supply	12 V supply not used on UDIMMs.
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE 2.5V or 3.3V.
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

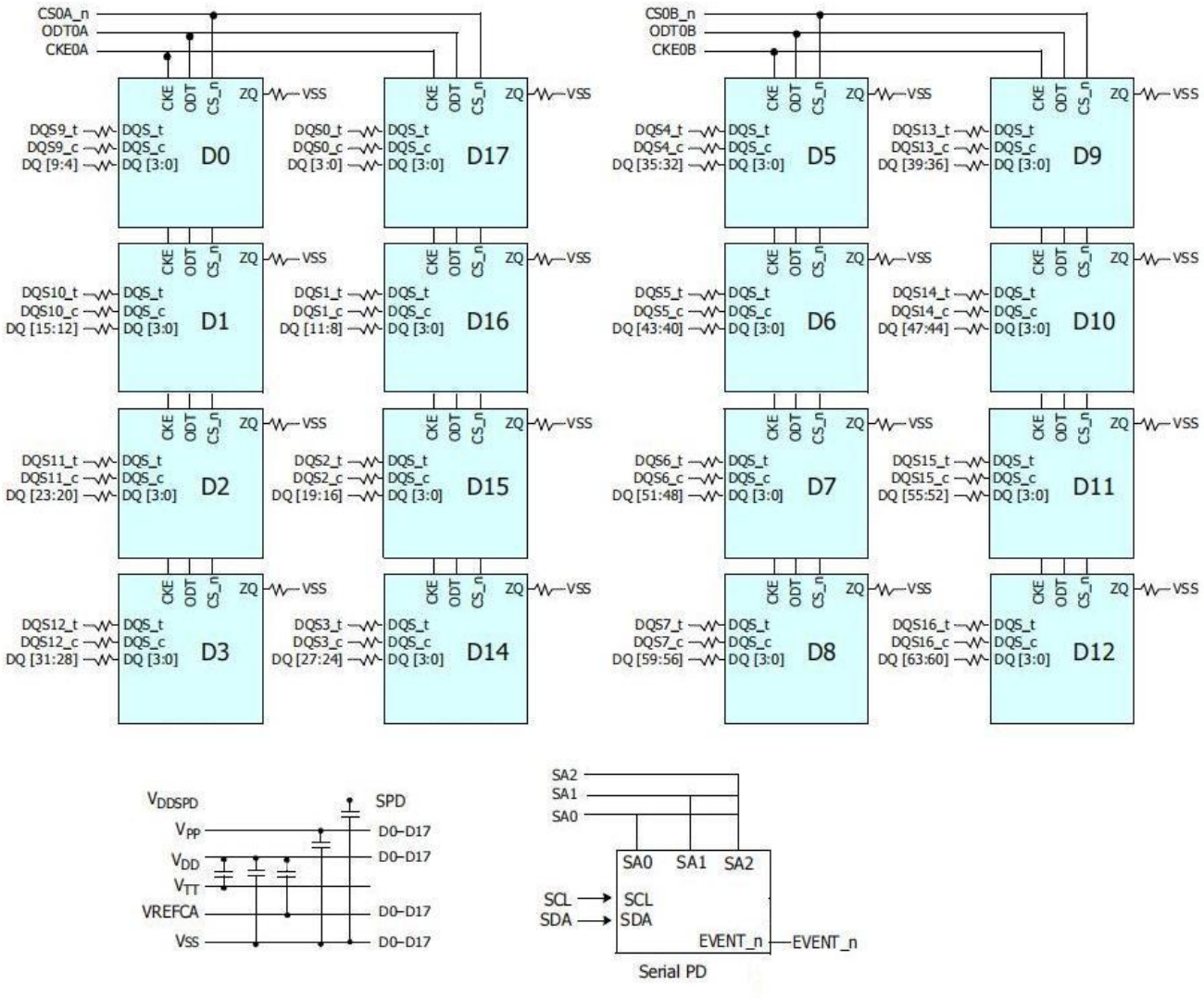
8. DQ MAPS

[Table 6] Component-to-Module DQ Map (R/C-A2)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	3	0	5	U2	3	8	16
	1	1	150		1	9	161
	2	2	12		2	10	23
	0	3	157		0	11	168
	7	4	3		7	12	14
	5	5	148		5	13	159
	6	6	10		6	14	21
	4	7	155		4	15	166
U3	3	16	27	U4	3	24	38
	1	17	172		1	25	183
	2	18	34		2	26	45
	0	19	179		0	27	190
	7	20	25		7	28	36
	5	21	170		5	29	181
	6	22	32		6	30	43
	4	23	177		4	31	188
U5	3	32	97	U6	3	40	108
	1	33	242		1	41	253
	2	34	104		2	42	115
	0	35	249		0	43	260
	7	36	95		7	44	106
	5	37	240		5	45	251
	6	38	102		6	46	113
	4	39	247		4	47	258
U7	3	48	119	U8	3	56	130
	1	49	264		1	57	275
	2	50	162		2	58	137
	0	51	271		0	59	282
	7	52	117		7	60	128
	5	53	262		5	61	273
	6	54	124		6	62	135
	4	55	269		4	63	280

9. FUNCTION BLOCK DIAGRAM

UDIMM



Note:

1. Unless otherwize noted, resistor values are 15Ω±5%.
2. ZQ resistors are 240Ω±1%.For all other resistor values refer to the appropriate wiring diagram.
3. VDD and VDDSPD also connect to the register. TEN pin of SDRAMs is tied to VSS.

10 ABSOLUTE MAXIMUM RATINGS

[Table 7] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	StorageTemperature	-55 to +100	℃	1,2

NOTE :

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affectreliability
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4) VPP must be equal or greater than VDD/VDDQ at all times.

11 AC & DC OPERATING CONDITIONS

[Table 8]Recommended DC Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltagecommand/ addressbus	0.49 ×V_{DD}	0.5 × V_{DD}	0.51 ×V_{DD}	V	3
I_{VTT}	Termination reference current from V_{TT}	–750	–	750	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_{IN}	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	–2.0	–	2.0	µA	5
I_{ZQ}	Input leakage current; ZQ	–3	–	3.0	µA	5, 6
I_{OZpd}	Output leakage current; V_{OUT} = V_{DD}; DQ is disabled	–	–	5.0	µA	
I_{OZpu}	Output leakage current; V_{OUT} = V_{SS}; DQ is disabled; ODT is disabled with ODT input HIGH	–	–	5.0	µA	
I_{VREFCA}	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	–2.0	–	2.0	µA	5

Notes:
1. V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

[Table 9] Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	Commercial operating casetemperature	0 to 85	°C	1, 2, 3
T_C		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to 85	°C	5
T_{OPER}	Extended temperature operating range (optional)	>85 to 95	°C	5
T_{STG}	Non-operating storage temperature	–55 to 100	°C	6
RH_{STG}	Non-operating Storage Relative Humidity (non-condensing)	5 to 95	%	
NA	Change Rate of Storage Temperature	20	°C/hour	

Notes:
1. Maximum operating case temperature; TC is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < T_{OPER} ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

12 SPD EEPROM OPERATING CONDITIONS

[Table 10] SPD EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{DDSPD}	–	2.5	–	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.5	–	$V_{DDSPD} \times 0.3$	V
Input high voltage: logic 1; all inputs	V_{IH}	$V_{DDSPD} \times 0.7$	–	$V_{DDSPD}+0.5$	V
Output low voltage: 3mA sink current V_{DDSPD} > 2V	V_{OL}	–	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	I_{LI}	–	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	I_{LO}	–	–	±5	µA

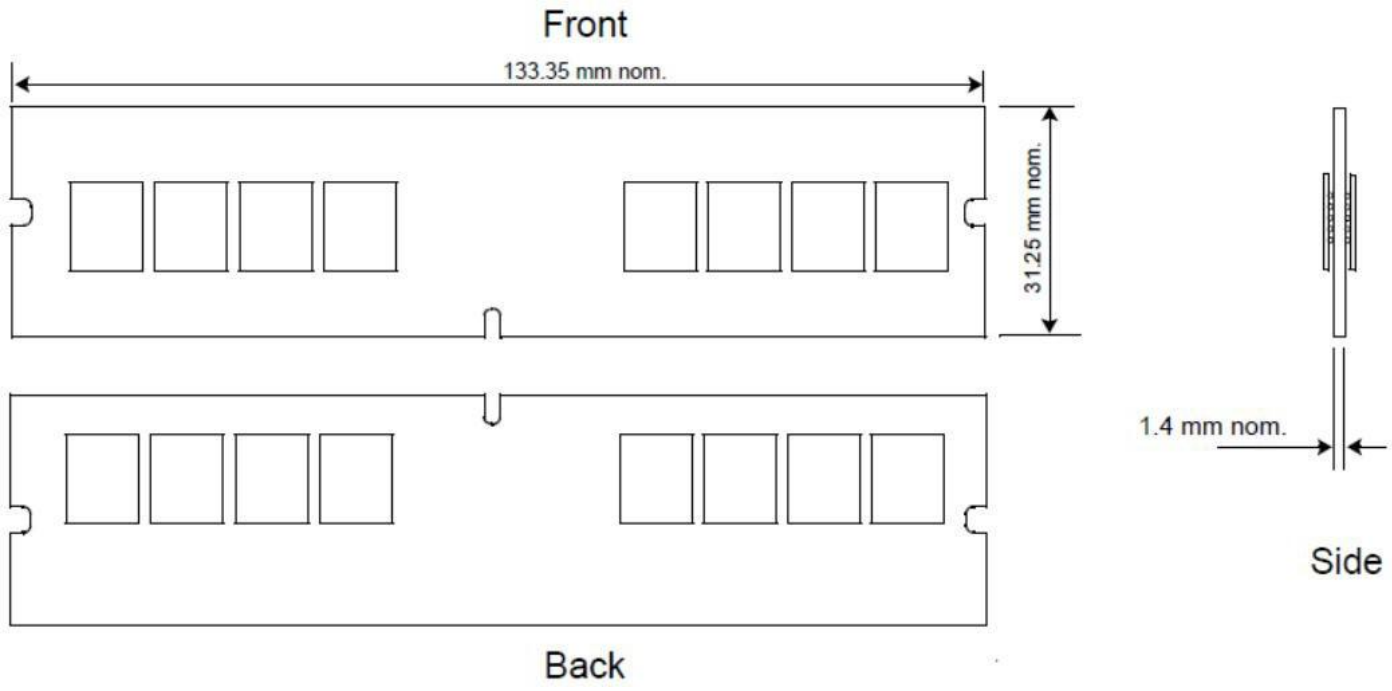
Notes: 1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
2. All voltages referenced to V_{DDSPD}.

[Table 11] SPD EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	t_{SCL}	10	1000	kHz
Clock pulse width HIGH time	t_{HIGH}	260	–	ns
Clock pulse width LOW time	t_{LOW}	500	–	ns
Detect clock LOW timeout	$t_{TIMEOUT}$	25	35	ms
SDA rise time	t_R	–	120	ns
SDA fall time	t_F	–	120	ns
Data-in setup time	$t_{SU:DAT}$	50	–	ns
Data-in hold time	$t_{HD:DI}$	0	–	ns
Data out hold time	$t_{HD:DAT}$	0	350	ns
Start condition setup time	$t_{SU:STA}$	260	–	ns
Start condition hold time	$t_{HD:STA}$	260	–	ns
Stop condition setup time	$t_{SU:STO}$	260	–	ns
Time the bus must be free before a new transition can start	t_{BUF}	500	–	ns
Write time	t_W	–	5	ms
Warm power cycle time off	t_{POFF}	1	–	ms
Time from power on to first command	t_{INIT}	10	–	ms

Note: 1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

13. PHYSICAL DIMENSIONS



P/N Decoder