DDR5 SDRAM SODIMM

TG5AA8G7LSFAWM-CG

DESCRIPTION

This document describes tyniGO's DDR5 1024M x 64 one rank 8GB DDR5-4800 CL40 1.1V SDRAM Small Outline DIMM product.

The produt is based on 4C 1024M x16-bit DDR5 FBGA components. The SPD is programmed follow JEDEC standard for 4800Mbps timing of 40-39-39 at 1.1V low power.

This product design specification reference JEDEC standard(JEDEC Standard No. 79-5)

This 262-pin SODIMM uses gold contact fingers and requires +1.1V power supply .

Ordering Information

Memory Type	Density	Organization	Component Composition	#of ranks
TG5AA8G7LSFAWM-CG	8GB	1024Mx64bit	DDR5 1024M*16 4C	1

Reference ONLY

Features

- DRAM VDD/VDDQ = 1.1V (-33mV / +67mV)
- DRAM VPP = 1.8V (–54mV / +108mV)
- 32 Bank with x4/x8
- 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Temperature Encoding
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Package Output Driver Test Mode
- Training Modes:
    - VrefDQ / VrefCA / VrefCS Training
    - Read Training Mode
    - CA Training Mode
    - CS Training Mode
    - Per Pin VREFDQ Training
    - Write Leveling Training Mode
    - Duty Cycle Adjuster (DCA) for Read - Global
    - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)
- sPPR Do / Undo / Lock
- MBIST / mPPR
- 0.5*CK Write Levling Internal Cycle Alignment
- Partial Array Self Refresh (PASR)
- NOT supported Adaptive Refresh Management (ARFM)
- NOT supported Refresh Interval Rate Indicator
- NOT required RFM

Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target CL- tRCD-tRP	tRCD-(ns)	tRC (ns)	tRP (ns)
4800	4800	40-40-40	16.666	48.00	16.666

Addressing

Configuration	1024Meg x 16
# BG / # Banks per BG / # Banks	4 / 4 / 16
Bank group address	BG0-BG1
Bank address in bank group	BA0-BA1
Row address	R0-R15
Column address	C0-C9
Page size	2KB

DDR5 SDRAM X16 Ballout

	1	2	3	4	5	6	7	8	9	
A	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	A
B	VDD	VDDQ	DQU2				DQU3	VDDQ	VDD	B
C	VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS	C
D	VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ	D
E	VDD	DQU4	DQU6				DQU7	DQU5	VDD	E
F	VDD	VDDQ	DQL2				DQL3	VDDQ	VDD	F
G	VSS	DQL0	DQSL_t				DML_n	DQL1	VSS	G
H	VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ	H
J	VDD	DQL4	DQL6				DQL7	DQL5	VDD	J
K	VSS	VDDQ	VSS				VSS	VDDQ	VSS	K
L	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	L
M	ALERT_n	VSS	CS_n				CK_c	VSS	VDD	M
N	VDDQ	CA4	CA0				CA1	CA5	VDDQ	N
P	VDD	CA6	CA2				CA3	CA7	VDD	P
R	VDDQ	VSS	CA8				CA9	VSS	VDDQ	R
T	CAI	CA10	CA12				CA13	CA11	RESET_n	T
U	VDD	VSS	VDD				VPP	VSS	VDD	U

Pin Assignments

262-Pin DDR5 SODIMM Front						262-Pin DDR5 SODIMM Back					
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	89	VSS	175	CB3_B	2	HSA	90	VSS	176	CB2_B
3	VIN_BULK	91	DQ30_A	177	VSS	4	HSCL	92	DQ31_A	178	VSS
5	RFU	93	VSS	179	DQ0_B	6	HSDA	94	VSS	180	DQ1_B
7	PWR_GOOD	95	CB0_A	181	VSS	8	PWR_EN	96	CB1_A	182	VSS
9	VSS	97	VSS	183	DQ2_B	10	VSS	98	VSS	184	DQ3_B
11	DQ0_A	99	CB2_A	185	VSS	12	DQ1_A	100	DQS4_A_c	186	VSS
13	VSS	101	VSS	187	DM0_B_n	14	VSS	102	DQS4_A_t	188	DQS0_B_c
15	DQ2_A	103	CB3_A	189	VSS	16	DQ3_A	104	VSS	190	DQS0_B_t
17	VSS	105	VSS	191	DQ4_B	18	VSS	106	CS0_A_n	192	VSS
19	DM0_A_n	107	CA0_A	193	VSS	20	DQS0_A_	108	ALERT_n	194	DQ5_B
21	VSS	109	CA1_A	195	DQ6_B	22	DQS0_A_	110	CS1_A_n	196	VSS
23	DQ4_A	111	VSS	197	VSS	24	VSS	112	VSS	198	DQ7_B
25	VSS	113	CA2_A	199	DQ8_B	26	DQ5_A	114	CA3_A	200	VSS
27	DQ6_A	115	CA4_A	201	VSS	28	VSS	116	CA5_A	202	DQ9_B
29	VSS	117	VSS	203	DQ10_B	30	DQ7_A	118	VSS	204	VSS
31	DQ8_A	119	CA6_A	205	VSS	32	VSS	120	CA7_A	206	DQ11_B
33	VSS	121	CA8_A	207	DQS1_B_c	34	DQ09_A	122	CA9_A	208	VSS
35	DQ10_A	123	VSS	209	DQS1_B_t	36	VSS	124	VSS	210	DM1_B_n
37	VSS	125	CA10_A	211	VSS	38	DQ11_A	126	CA11_A	212	VSS
39	DQS1_A_c	KEY		213	DQ12_B	40	VSS	KEY		214	DQ13_B
41	DQS1_A_t	127	CA12_A	215	VSS	42	DM1_A_n	128	RFU	216	VSS
43	VSS	129	VSS	217	DQ14_B	44	VSS	130	VSS	218	DQ15_B
45	DQ12_A	131	CK0_A_t	219	VSS	46	DQ13_A	132	CK1_A_t	220	VSS
47	VSS	133	CK0_A_c	221	DQ16_B	48	VSS	134	CK1_A_c	222	DQ17_B
49	DQ14_A	135	VSS	223	VSS	50	DQ15_A	136	VSS	224	VSS
51	VSS	137	CK0_B_t	225	DQ18_B	52	VSS	138	CK1_B_t	226	DQ19_B
53	DQ16_A	139	CK0_B_c	227	VSS	54	DQ17_A	140	CK1_B_c	228	VSS
55	VSS	141	VSS	229	DM2_B_n	56	VSS	142	VSS	230	DQS2_B_c
57	DQ18_A	143	RFU	231	VSS	58	DQ19_A	144	CA12_B	232	DQS2_B_t
59	VSS	145	CA11_B	233	DQ20_B	60	VSS	146	CA10_B	234	VSS
61	DM2_A_n	147	VSS	235	VSS	62	DQS2_A_c	148	VSS	236	DQ21_B
63	VSS	149	CA9_B	237	DQ22_B	64	DQS2_A_t	150	CA8_B	238	VSS
65	DQ20_A	151	CA7_B	239	VSS	66	VSS	152	CA6_B	240	DQ23_B
67	VSS	153	VSS	241	DQ24_B	68	DQ21_A	154	VSS	242	VSS
69	DQ22_A	155	CA5_B	243	VSS	70	VSS	156	CA4_B	244	DQ25_B
71	VSS	157	CA3_B	245	DQ26_B	72	DQ23_A	158	CA2_B	246	VSS
73	DQ24_A	159	VSS	247	VSS	74	VSS	160	VSS	248	DQ27_B
75	VSS	161	CS0_B_n	249	DQS3_B_c	76	DQ25_A	162	CA1_B	250	VSS
77	DQ26_A	163	RESET_n	251	DQS3_B_t	78	VSS	164	CA0_B	252	DM3_B_n
79	VSS	165	CS1_B_n	253	VSS	80	DQ27_A	166	VSS	254	VSS
81	DQS3_A_c	167	VSS	255	DQ28_B	82	VSS	168	CB0_B	256	DQ29_B
83	DQS3_A_t	169	DQS4_B_c	257	VSS	84	DM3_A_n	170	VSS	258	VSS
85	VSS	171	DQS4_B_t	259	DQ30_B	86	VSS	172	CB1_B	260	DQ31_B
87	DQ28_A	173	VSS	261	VSS	88	DQ29_A	174	VSS	262	VSS

Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DM_n, DMU_n, DML n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA [13:0]	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ ,
DQ	Input / Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
ALERT n	Input/Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input.Using this signal or not is dependent on system. In case of not connected as Signal,ALERT_n Pin must be bounded to V DDQ on board.
TEN	Input	Connectivity Test Mode Enable: Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of V DDQ. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.

MIR	Input	Mirror: Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSSQ if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected to VDDQ
CAI	Input	Command & Address Inversion: With the CAI pin connected to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSSQ if no CA inversion is required.
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected to VSS and apply Group B settings if the pin is connected to V DDQ.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V +/- 0.055 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.1 V +/- 0.055 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V Nom, 1.71V Min, 1.98V Max
ZQ	Supply	Reference Pin for ZQ calibration
NOTES:		

Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V	1,3
VPP	Voltage on VPPpin relative toVss	-0.3 ~ 2.1	V	4
VIN, VOUT	Voltage on any pin relative toVss	-0.3 ~ 1.4	V	1,3,5
TSTG	Storage Temperature	-55 to +100	°C	1,2

Note(s):

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-
2 standard.

3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV

4. VPP must be equal or greater than VDD/VDDQ at all times.

5.Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

DRAM Component Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit: °C)		Grade	Notes
		Min	Max		
T_{oper_normal}	Normal Operating Temperature	0	85	NT	1,2,3,4
$T_{oper\_extended}$	Extended Operating Temperature	0	95	XT	1,2,3,4

Note(s):

1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.

2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3. All DDR5 SDRDAMs are required to operate in NT and XT temperature ranges.

4. When operating above 85°C, the host shall provide appropriate Refresh mode controls associated with the increased temperature range . The full description of these settings are defined in Table 68 in section 4.13.5

5. Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.

DDR5-4800 Speed Bins and Operations

Speed Bin					**DDR5-4800**							**Unit**	**NOTE**
CL-nRCD-nRP					**40-40-40**								
Parameter				**Symbol**	**min**				**max**				
Read command to first data				tAA	16.666				22.222			ns	12
Activate to Read or Write command delay time				tRCD	16.666				-			ns	7
Row Precharge Time				tRP	16.666				-			ns	7
Activate to Precharge command period				tRAS	32				5 x tREFI1			ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.666				-			ns	7,8
CAS Write Latency				CWL	CL-2							nCK	
Speed Bins	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins									
4800	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED	ns	
Supported CL					22,24,26,28,30,32,34,36,40,42		22,26,28,30,32,36,40,42		22,28,30,32,36,40,42		22,28,32,36,40,42	nCK	

PCB

General

* Board size：69.6±0.1x30.0±0.15mm
* Thickness： 1.20±0.1mm
* Panel：6 pieces PCB per panel
* 8-layer board
* Pin count：262 PIN

PCB Material

* Halogen Free

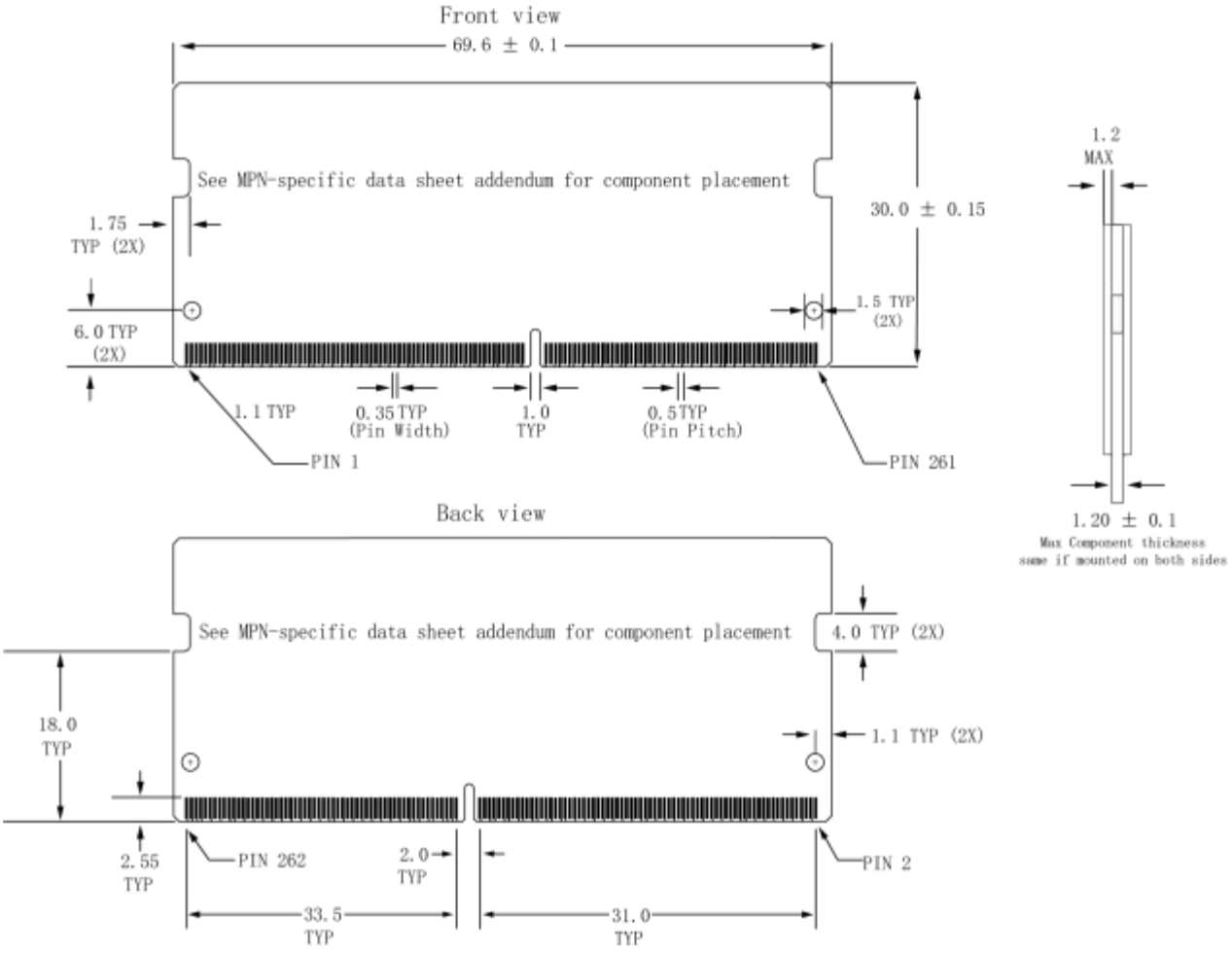
Plating

*Edge Connector Plating: Nickel Followed by gold
Nickel Plating Thickness: 120 u" min.
Surface treatment:
Gold Plating: 3u" min
SMT PAD: average 2~3u".

Reference:

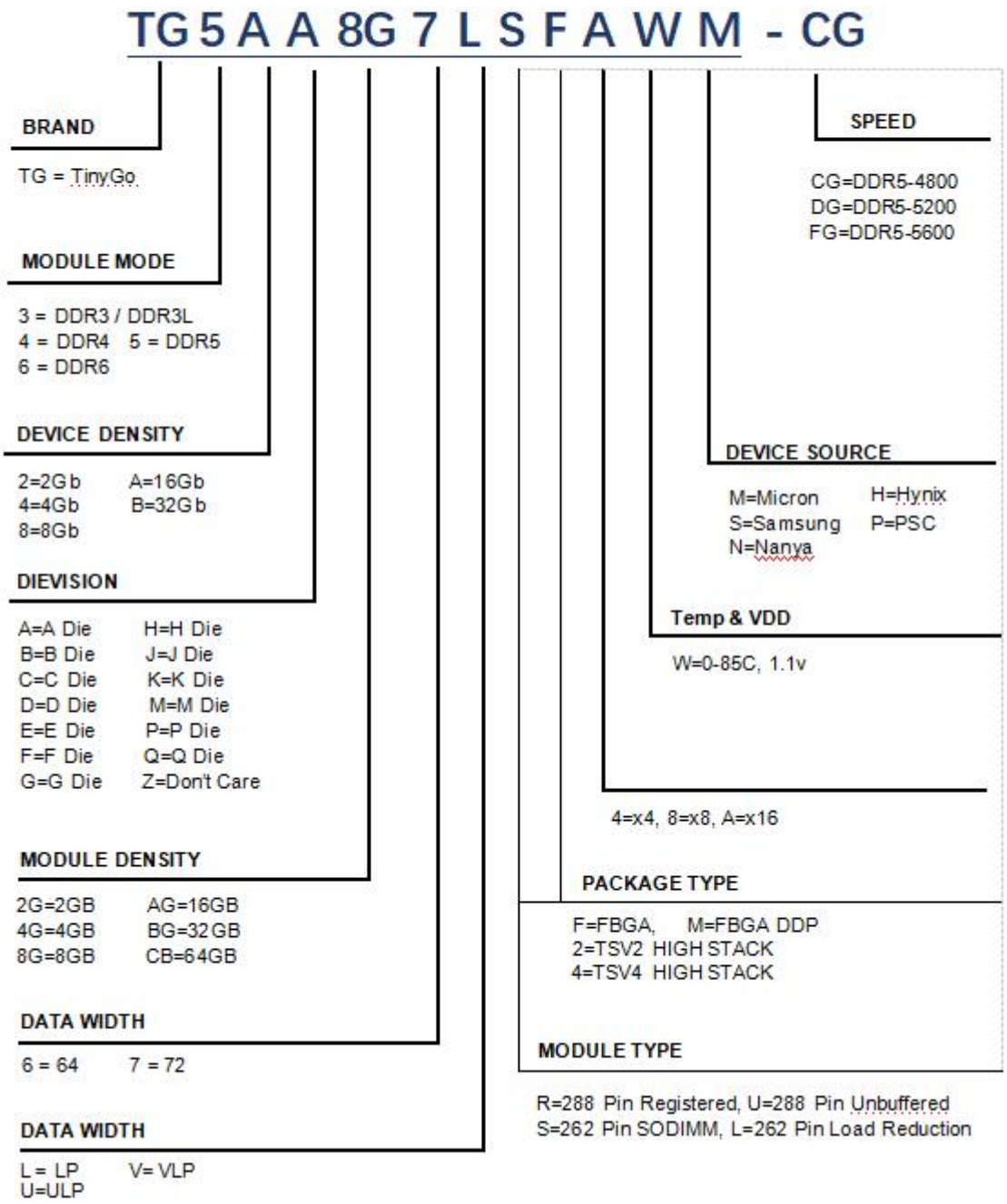
Raw Card	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# Address bits row/col
/	8GB	1Gx64	16Gbit	1024Mx16	4	1	FBGA	16/10

Module Dimensions



Notes:
1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
2. Tolerance on all dimensions ±0.15 unless otherwise specified.
3. The dimensional diagram is for reference only.

P/N Decoder


TG5AA8G7LSFAWM-CG
BRAND
TG = TinyGo
MODULE MODE
3 = DDR3 / DDR3L
4 = DDR4 5 = DDR5
6 = DDR6
DEVICE DENSITY
2=2Gb A=16Gb
4=4Gb B=32Gb
8=8Gb
DIEVISION
A=A Die H=H Die
B=B Die J=J Die
C=C Die K=K Die
D=D Die M=M Die
E=E Die P=P Die
F=F Die Q=Q Die
G=G Die Z=Don't Care
MODULE DENSITY
2G=2GB AG=16GB
4G=4GB BG=32GB
8G=8GB CB=64GB
DATA WIDTH
6 = 64 7 = 72
DATA WIDTH
L = LP V= VLP
U=ULP
MODULE TYPE
R=288 Pin Registered, U=288 Pin Unbuffered
S=262 Pin SODIMM, L=262 Pin Load Reduction
PACKAGE TYPE
F=FBGA, M=FBGA DDP
2=TSV2 HIGH STACK
4=TSV4 HIGH STACK
4=x4, 8=x8, A=x16
Temp & VDD
W=0-85C, 1.1v
DEVICE SOURCE
M=Micron H=Hynix
S=Samsung P=PSC
N=Nanya
SPEED
CG=DDR5-4800
DG=DDR5-5200
FG=DDR5-5600