DDR4 SODIMM

BASE ON 8GB

TG44Z8G6LSF4NS-AF

REVISION HISTORY

Revision No.	History	Draft Date	Editor
1.0	Initial Release	2025.07.22	Yang

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1. FEATURES

- 260-pin, Unbuffered Small Outline Dual In-line memory module (SODIMM)
- Fast data transfer rates: 2400MHz/2666MHz/3200Mbps
- 8GB (1024M x1x64)
- VDD = 1.20V (NOM)
- VPP = 2.5V (NOM)
- VDDSPD = 2.5V (NOM)
- Nominal and dynamic on-die termination(ODT)
- Programmable Partial Array Self-Refresh (PASR)
- Data bus inversion (DBI) for data bus
- On-die VREFDQ generation and calibration
- Single-Rank
- On-board I^2C serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- RoHS compliant
- Fly-by topology
- Terminated control command and address bus
- Commercial (0°C ≤ TOPER ≤ 70°C)
- 0.83ns@ CL =17 (DDR4-2400)/0.75ns@ CL =19 (DDR4-2666)/0.625ns@ CL =24 (DDR4-3200)

2. DDR4 UNBUFFERED SODIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Number of Rank	Organization	Density	Data Rate	Temp Sensor	Height	Environment
1	1Gx1x64（1Rx4）	8GB	2400 Mbps	No	30mm	Commercial
1	1Gx1x64（1Rx4）	8GB	2666 Mbps	No	30mm	Commercial
1	1Gx1x64（1Rx4）	8GB	3200 Mbps	No	30mm	Commercial

3. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	17-17-17	19-19-19	21-21-21	24-22-22	
tCK(min)	0.833	0.75	0.682	0.625	ns
CAS Latency	17	19	21	24	nCK
tRCD(min)	14.16	14.25	14.32	13.75	ns
tRP(min)	14.16	14.25	14.32	13.75	ns
tRAS(min)	32	32	32	32	ns
tRC(min)	46.16	46.25	46.32	45.75	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- VDDQ = 1.2V ± 0.06V
- Bi-directional Differential Data Strobe
- Average Refresh Period: 7.8 μs at 0° C ≤ TCase ≤ 85° C; 3.9 μs at 85° C < TCase ≤ 95° C.

4. ADDRESS CONFIGURATION

[Table 3] address configuration

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
1024Mx4(4Gb)	A0-A15	A0-A9	BG0-BG1	BA0-BA1	A10/AP

5. UNBUFFERED SODIMM PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	79	DQ30	80	DQ31	157	CS1_n1	158	A13	235	VSS	236	DQ57
3	DQ5	4	DQ4	81	VSS	82	VSS	159	VDD	160	VDD	237	DQ56	238	VSS
5	VSS	6	VSS	83	DQ26	84	DQ27	161	ODT1	162	C0,CS2_n,NC	239	VSS	240	DQS7_c
7	DQ1	8	DQ0	85	VSS	86	VSS	163	VDD	164	VREFCA	241	DM7_n/ DBI7_n	242	DQS7_t
9	VSS	10	VSS	87	CB5,NC	88	CB4,NC	165	C1,CS3_n, NC	166	SA2	243	VSS	244	VSS
11	DQS0_c	12	DM0_n/ DBI0_n	89	VSS	90	VSS	167	VSS	168	VSS	245	DQ62	246	DQ63
13	DQS0_t	14	VSS	91	CB1,NC	92	CB0,NC	169	DQ37	170	DQ36	247	VSS	248	VSS
15	VSS	16	DQ6	93	VSS	94	VSS	171	VSS	172	VSS	249	DQ58	250	DQ59
17	DQ7	18	VSS	95	DQS8_c	96	DBI8_n	173	DQ33	174	DQ32	251	VSS	252	VSS
19	VSS	20	DQ2	97	DQS8_t	98	VSS	175	VSS	176	VSS	253	SCL	254	SDA
21	DQ3	22	VSS	99	VSS	100	CB6,NC	177	DQS4_c	178	DM4_n/ DBI4_n	255	VDDSPD	256	SA0
23	VSS	24	DQ12	101	CB2,NC	102	VSS	179	DQS4_t	180	VSS	257	VPP	258	Vtt
25	DQ13	26	VSS	103	VSS	104	CB7,NC	181	VSS	182	DQ39	259	VPP	260	SA1
27	VSS	28	DQ8	105	CB3,NC	106	VSS	183	DQ38	184	VSS				
29	DQ9	30	VSS	107	VSS	108	RESET_n	185	VSS	186	DQ35				
31	VSS	32	DQS1_c	109	CKE0	110	CKE1	187	DQ34	188	VSS				
33	DM1_n/ DBI1_n	34	DQS1_t	111	VDD	112	VDD	189	VSS	190	DQ45				
35	VSS	36	VSS	113	BG1	114	ACT_n	191	DQ44	192	VSS				
37	DQ15	38	DQ14	115	BG0	116	ALERT_n	193	VSS	194	DQ41				
39	VSS	40	VSS	117	VDD	118	VDD	195	DQ40	196	VSS				
41	DQ10	42	DQ11	119	A12	120	A11	197	VSS	198	DQS5_c				
43	VSS	44	VSS	121	A9	122	A7	199	DM5_n/ DBI5_n	200	DQS5_t				
45	DQ21	46	DQ20	123	VDD	124	VDD	201	VSS	202	VSS				
47	VSS	48	VSS	125	A8	126	A5	203	DQ46	204	DQ47				
49	DQ17	50	DQ16	127	A6	128	A4	205	VSS	206	VSS				
51	VSS	52	VSS	129	VDD	130	VDD	207	DQ42	208	DQ43				
53	DQS2_c	54	DM2_n/ DBI2_n	131	A3	132	A2	209	VSS	210	VSS				
55	DQS2_t	56	VSS	133	A1	134	EVENT_n	211	DQ52	212	DQ53				
57	VSS	58	DQ22	135	VDD	136	VDD	213	VSS	214	VSS				
59	DQ23	60	VSS	137	CK0_t	138	CK1_t	215	DQ49	216	DQ48				
61	VSS	62	DQ18	139	CK0_c	140	CK1_c	217	VSS	218	VSS				
63	DQ19	64	VSS	141	VDD	142	VDD	219	DQS6_c	220	DM6_n/ DBI6_n				
65	VSS	66	DQ28	143	Parity	144	A0	221	DQS6_t	222	VSS				
67	DQ29	68	VSS	145	BA1	146	A10/AP	223	VSS	224	DQ54				
69	VSS	70	DQ24	147	VDD	148	VDD	225	DQ55	226	VSS				
71	DQ25	72	VSS	149	CS0_n	150	BA0	227	VSS	228	DQ50				
73	VSS	74	DQS3_c	151	A14/ WE_n	152	A16/ RAS_n	229	DQ51	230	VSS				
75	DM3_n/ DBI3_n	76	DQS3_t	153	VDD	154	VDD	231	VSS	232	DQ60				
77	VSS	78	VSS	155	ODT0	156	A15/ CAS_n	233	DQ61	234	VSS				

6. PIN DESCRIPTION

[Table 4] pin description

Pin Name	Description
A0–A16	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n1)	SDRAM row address strobe
CAS_n2)	SDRAM column address strobe
WE_n3)	SDRAM write enable
CS0_n–CS1_n	Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	Register on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS8_t	SDRAM data strobes
	(positive line of differential pair)
DQS0_c–	SDRAM data strobes
DQS8_c	(negative line of differential pair)
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x4-based x72 DIMMs)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
Pin Name	Description
SCL	I2C serial bus clock for SPD/TS
SDA	I2C serial bus data line for SPD/TS
SA0~SA2	I2C slave address select for SPD/TS
PARITY	SDRAM parity input
VDD	SDRAM I/O & core power supply
VPP	SDRAM activating power supply
C0,C1	Chip ID lines for 3DS components
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	SDRAM ALERT_n
RESET_n	Set SDRAMs to a Known State
EVENT_n	TS signals a thermal event has occurred
VTT	Termination supply for the Address, Command and Control bus
NC	No connection

NOTE :

1) RAS_n is a multiplexed function with A16.
2) CAS_n is a multiplexed function with A15.
3) WE_n is a multiplexed function with A14.

7. INPUT/OUTPUT FUNCTIONAL DESCRIPTION

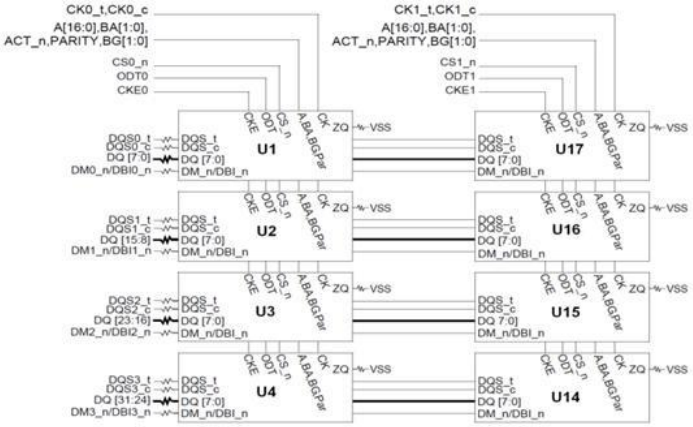
[Table 5] Input/Output function description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initializationsequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintainedhigh throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal tothe DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x4 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/ output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X4
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0

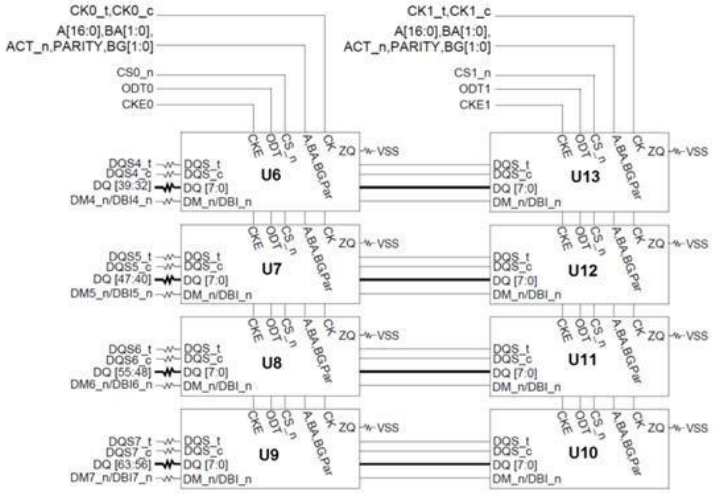
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/ BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bankis selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the- fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table fordetails.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_nis HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ isused.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered inwrite data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not supportsingle-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x4 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/ TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A17-A0, and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.

ALERT_n	Input/ Output	Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

8. FUNCTION BLOCK DIAGRAM



Note 1: Unless otherwise noted, resistor values are 15 Ω ± 5%.
Note 2: ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.



Note 1: Unless otherwise noted, resistor values are 15 Ω ± 5%.
Note 2: ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram..
Note 3: EVENT_n is not wired on this design.

9. ABSOLUTE MAXIMUM RATINGS

[Table 8] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	StorageTemperature	-55 to +100	℃	1,2

NOTE :

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affectreliability
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4) VPP must be equal or greater than VDD/VDDQ at all times.

10. AC & DC OPERATING CONDITIONS

[Table 9] Recommended DC Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltagecommand/ addressbus	0.49 ×V_{DD}	0.5 × V_{DD}	0.51 ×V_{DD}	V	3
I_{VTT}	Termination reference current from V_{TT}	–750	–	750	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_{IN}	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	–2.0	–	2.0	µA	5
I_{ZQ}	Input leakage current; ZQ	–3	–	3.0	µA	5, 6
I_{OZpd}	Output leakage current; V_{OUT} = V_{DD}; DQ is disabled	–	–	5.0	µA	
I_{OZpu}	Output leakage current; V_{OUT} = V_{SS}; DQ is disabled; ODT is disabled with ODT input HIGH	–	–	5.0	µA	
I_{VREFCA}	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	–2.0	–	2.0	µA	5

Notes:
1. V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

[Table 10] DRAM Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
TC	Commercial operating casetemperature	0 to 85	°C	1, 2, 3
TC		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to 85	°C	5
T_{OPER}	Extended temperature operating range (optional)	>85 to 95	°C	5
T_{STG}	Non-operating storage temperature	–55 to 100	°C	6
RH_{STG}	Non-operating Storage Relative Humidity (non-condensing)	5 to 95	%	
NA	Change Rate of Storage Temperature	20	°C/hour	

Notes:
1. Maximum operating case temperature; TC is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < T_{OPER} ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

11. SPD EEPROM OPERATING CONDITIONS

[Table 11] SPD EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{DDSPD}	–	2.5	–	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.5	–	$V_{DDSPD} \times 0.3$	V
Input high voltage: logic 1; all inputs	V_{IH}	$V_{DDSPD} \times 0.7$	–	$V_{DDSPD} + 0.5$	V
Output low voltage: 3mA sink current V_{DDSPD} > 2V	V_{OL}	–	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	I_{LI}	–	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	I_{LO}	–	–	±5	µA

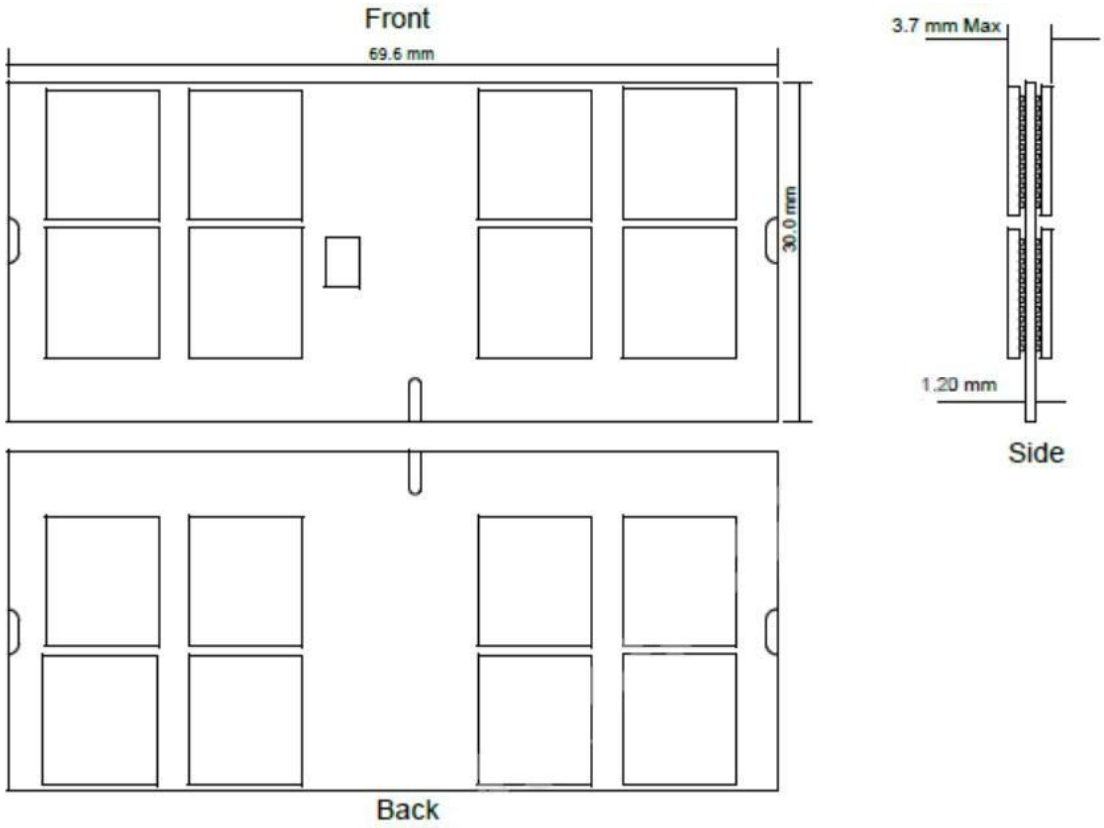
Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
2. All voltages referenced to V_{DDSPD}.

[Table 12] SPD EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	t_{SCL}	10	1000	kHz
Clock pulse width HIGH time	t_{HIGH}	260	–	ns
Clock pulse width LOW time	t_{LOW}	500	–	ns
Detect clock LOW timeout	$t_{TIMEOUT}$	25	35	ms
SDA rise time	t_R	–	120	ns
SDA fall time	t_F	–	120	ns
Data-in setup time	$t_{SU:DAT}$	50	–	ns
Data-in hold time	$t_{HD:DI}$	0	–	ns
Data out hold time	$t_{HD:DAT}$	0	350	ns
Start condition setup time	$t_{SU:STA}$	260	–	ns
Start condition hold time	$t_{HD:STA}$	260	–	ns
Stop condition setup time	$t_{SU:STO}$	260	–	ns
Time the bus must be free before a new transition can start	t_{BUF}	500	–	ns
Write time	t_W	–	5	ms
Warm power cycle time off	t_{POFF}	1	–	ms
Time from power on to first command	t_{INIT}	10	–	ms

Note:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

12. PHYSICAL DIMENSIONS



13. Part Number Decode

P/N Decoder